spread code generator **708** by detecting the peak of the cross-correlation series stored in the 2 port RAM **706** by the searcher correlator **705** with respect to the interpolation filter operation, power calculation, slot-to-slot averaging and the number of RAKE fingers and reading the de-spread signal written in the 2 port RAM by the data demodulation correlator **709**, combining at a maximum ratio (RAKE combination) by pilot symbol assisted coherent detecting the respective RAKE fingers and then deciding the reception data.

The searcher correlator **705**, spread code generator **708** and data demodulation correlator **709** can be formed by a hardware, for example, gate array (G/A), exclusive LSI, and the like. Assuming that the chip rate is set to 4.096 Mcps and the symbol rate to 256 ksps, the exclusive hardware may process the chip rate requiring simple and high-rate processing. While the DSP firmware may realize symbol rate processing requiring relatively a low rate but complex processing. As a result, the most desirable embodiment can be realized.

A first advantageous effect of the present invention is that the probability and accuracy for appropriately detecting the peak point of the delay profile can be improved even if the Eb/No per path is low. Therefore the appropriate reception timing can be always established, leading to the improved reception quality. Furthermore, as the present invention meets desired reception quality even under the lower Eb/No condition, the capacity of the cellular system using the CDMA and the cell radius covered by 1 base station can be enlarged.

As the first reason for the above-described effect provided by the present invention, the delay profile is provided by obtaining a cross-correlation between a known signal and the reception signal over a plurality of symbols or coherent adding over a plurality of symbols (normally the number of pilot symbols per slot). And then the power (sum of squares) is obtained. As a result, the power of the noise component contained in the cross-correlation value is reduced to 1/(number of pilot symbols), which is smaller than that of the prior art case. Assuming that the number of the pilot symbol per slot is 16, the power of the noise component can be reduced by about 12 dB.

As the second reason, since the same reception signal is repeatedly used for calculating the correlation value with different delays, the level relationship among cross-correlation values with different delays can be strictly maintained irrespective of large variation of the reception level owing to fading. Therefore, the present invention can completely solve such problem that the cross-correlation value obtained at a moment when the reception level is raised by fading exceeds the cross-correlation value of the correct peak point obtained at a moment when the reception level is low.

As the third reason, in the present invention, the cross-correlation value is obtained at 1/2 chip interval and then it is obtained at a shorter interval using an interpolation filter. Accordingly more accurate peak point (delay time) of the delay profile can be obtained. The present invention greatly improves the accuracy of detecting the reception timing without increasing processing amount.

A second advantageous effect of the present invention is that the operation amount required for obtaining the peak of the delay profile can be reduced.

This is because that the present invention requires to obtain the correlation value only at 1/2 interval in order to keep deterioration of the Eb/No required to an optimum reception timing to be 1 dB or less. While the prior art requires to obtain power of the correlation value at 1/4 interval. Since the noise contained in the cross-correlation value can be reduced, the number of averaging processings for restraining the dispersion of the noise power can also be decreased.

A third advantageous effect of the present invention is that the size of the hardware used for the base station system can be reduced.

This is because that as the circuit of the present invention realizes all functions of the initial sync. capture (initial search), new path capture (search) and sync. tracking by replacing two circuits, initial sync. capture circuit (search circuit) and sync. tracking circuit (for example, DLL (Delay Lock Loop)) that have been required to be equipped with the conventional system.

Referring to FIG. **1** and FIG. **9**, the power measurement section **107** and comparison section **108** are provided and the interpolation filter **103** is operated at a predetermined threshold value or more. However the objective of the present invention can be achieved by operating the interpolation filter **103** irrespective of the threshold value under no provision of the power measurement section **107** and comparison section **108**.

The entire disclosure of Japanese Patent Application No. 8-185103 filed on Jul. 15, 1996 including specification, claims, drawing and summary are incorporated herein by reference in its entirety.

What is claimed is:

1. A reception timing detection circuit of a CDMA receiver used for a mobile communication system using a direct spread code division multiple access method comprising:

correlation means for obtaining a cross-correlation between a reception signal and a known signal series periodically within a predetermined lag and outputting a cross-correlation signal indicating said obtained cross-correlation;

an interpolation filter for re-sampling said cross-correlation signal at a frequency higher than a sampling frequency for said cross-correlation signal and outputting said re-sampled cross-correlation signal;

power calculation means for calculating power of said re-sampled cross-correlation signal;

averaging means for averaging said calculated power of cross-correlation signal over a plurality of cycles; and

peak detection means for detecting a peak of said averaged power of cross-correlation signal and determining a timing at which said peak is detected as a reception timing.

2. The reception timing detection circuit of a CDMA receiver of claim **1**, wherein said known signal series is obtained by spreading a known pilot symbol inserted to said reception signal at predetermined period with a spread code.

3. The reception timing detection circuit of a CDMA receiver of claim **1**, wherein said known signal series is obtained by re-spreading a signal series produced by de-spreading said reception signal with a spread code.

4. The reception timing detection circuit of a CDMA receiver of claim **1**, wherein said correlation means comprises a matched filter that matches a series produced by spreading a known signal series with a spread code and time window means that allows a signal output from said matched filter to pass through within a predetermined period only.

5. The reception timing detection circuit of a CDMA receiver of claim **1**, wherein a cycle of a spread code is